Colonial

ELECTRONIC MANUFACTURERS, INCORPORATED

Design For Manufacturability

GUIDELINES

DFM-1 REV-C

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DFM-1 Rev -C
May 16, 2001

Design for Manufacturing Specification for Thru-Hole / Surface Mount Technology (All Dimensions in inches unless otherwise specified).

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Design For Manufacturing Specification
For Thru-Hole/Surface Mount Technology

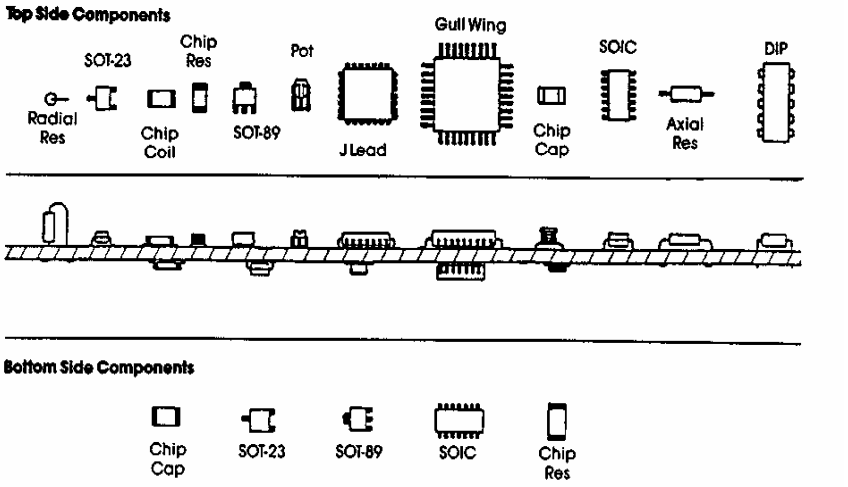
1.0 Introduction

1.1 Scope - This DFM Guideline establishes minimum criteria for the design and layout of single, double-sided, and multi-layer designs using through-hole, surface mount, or mixed technologies. For PWB's or also known as PCB's

1.2 Applicable Documents

IPC-T-50-Terms and Definitions
IPC-SM-782-Surface Mount Land Patterns
IPC-S-100-Standards Manual
IPC-D-330-Design Guide Manual
IPC-G-400-Guidelines Manual
IPC-D-275-Design Standard for Rigid Printed Boards and Assemblies
Current supplier standards as applicable for fabrication and assembly.

1.3 - Assembly Types



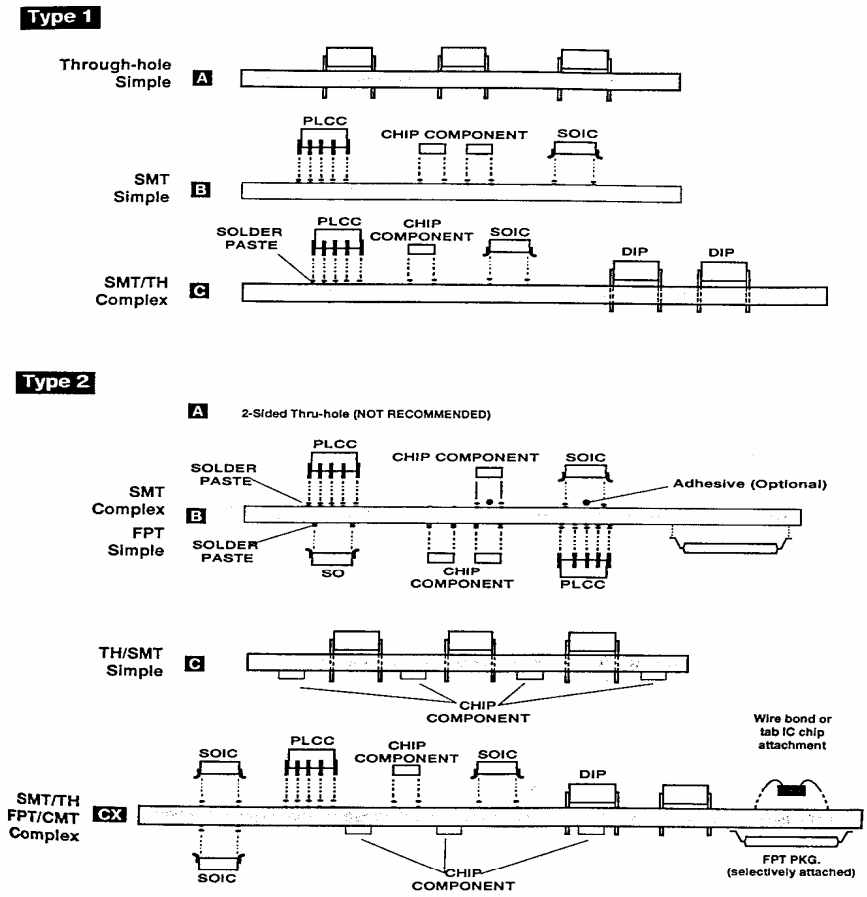
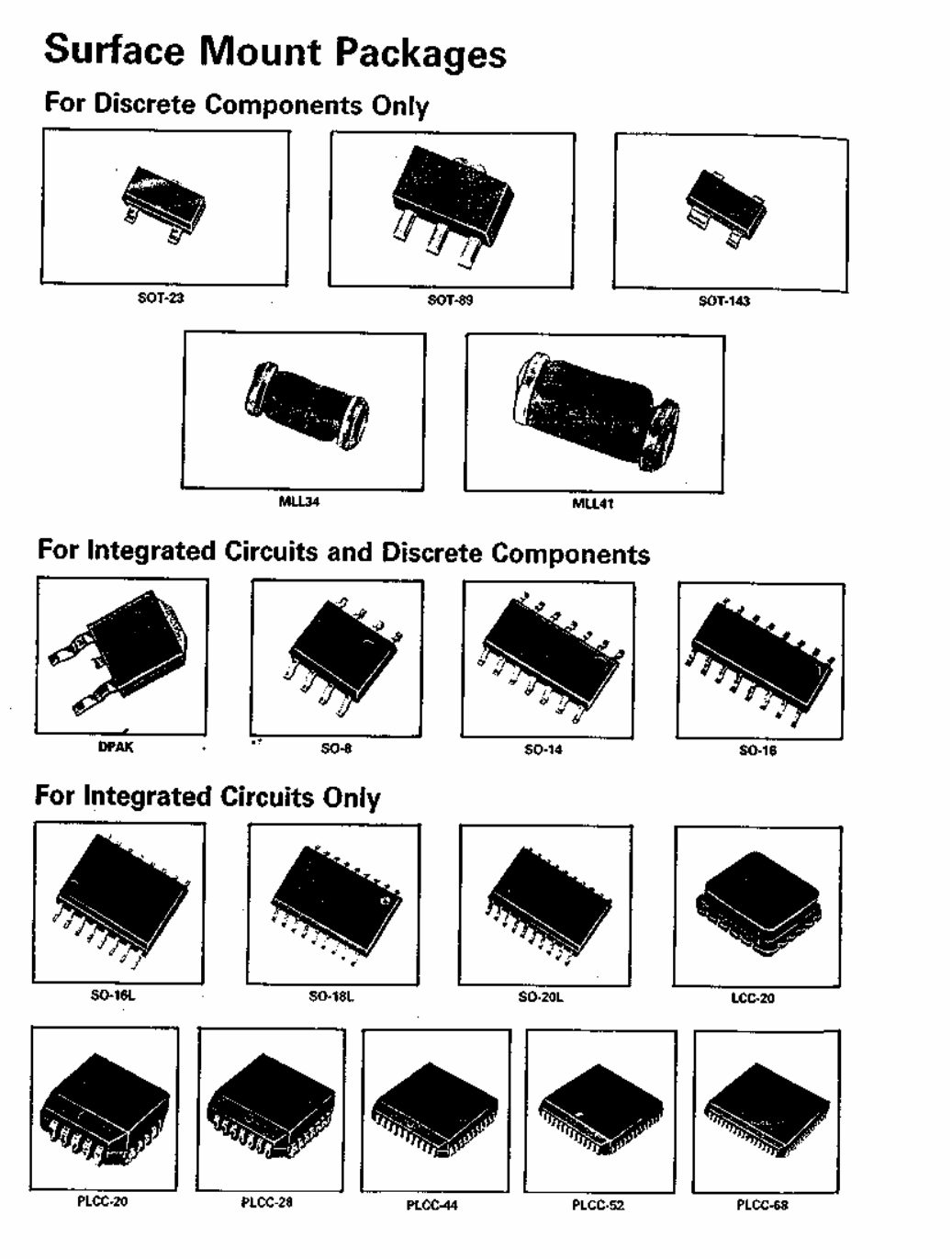


Figure 1.3 Assembly Types

1.4 – Surface Mount Packages



2.0 Basic PCB Design Requirements

2.1 Board Outline – The maximum board size is 18.00 long x 14.00 wide. The minimum panel size is 4.00 long x 2.50 wide.

2.2 Board Thickness – For standard PWB materials (Fr-4, G-10, Etc.)The minimum PWB thickness is .031 while the maximum is .125. The typical multi-layer PWB is .062 thick while the typical back-plane is 0.093 to 0.125 thick. Other materials are available to make PWB's of thinner materials such as metal or ceramic substrates, to go below the 0.031 minimum restrictions.

2.3 Bow and Twist – The maximum bow and twist after fabrication should be .010 in/in. All copper planes will be balanced. Outer layers to be cross – hatched for wave solder thermal characteristics to minimize warping.

2.4 Shape – The PWB or panel is required to have two parallel sides in the direction of process flow. See Figure 2.4. The leading edge of the board, which determines the process flow, should be the shortest edge of the board. The longest parallel edges of the board, should be the conveyor edges. The leading edge of the board should have a square edge. If the edge is not square it will exhibit a problem in the assembly process due to the board needing to contact a mechanical stop in the placement equipment, or for wave soldering consideration.

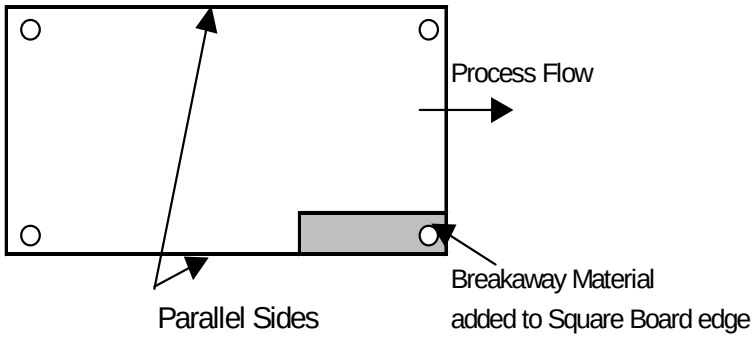


Figure 2.4: PWB Shape Board or Pallet

2.5 Placeable area (Through-Hole) – Tooling hole Clearances and placeable area requirements for through-hole DIPS and Axials

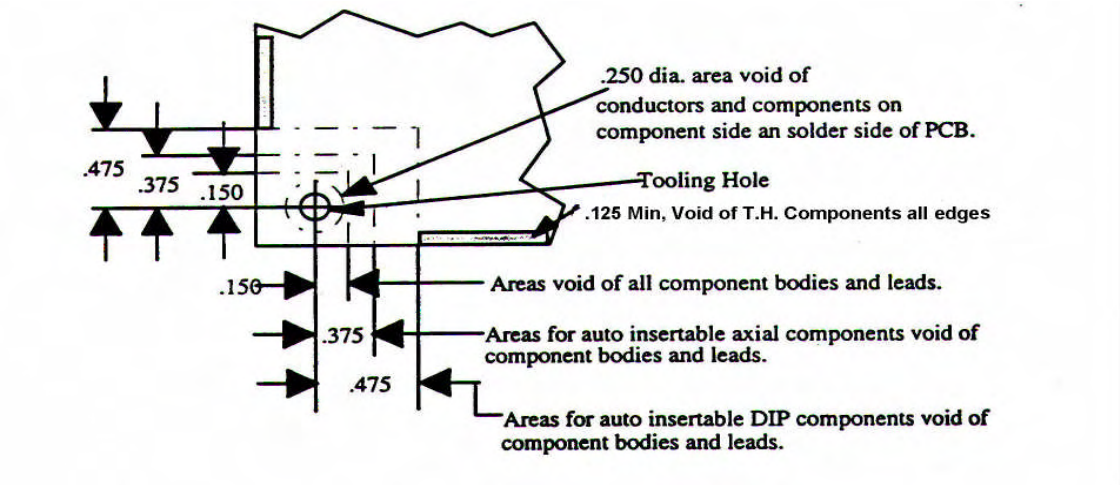


Figure 2.5:Tooling Hole and Edge Clearances for Through-Hole DIPS and Axials

2.6 Tooling Hole Locations – Four non-plated tooling holes 0.125" are required on each PWB in order to provide accuracy for automatic assembly and test processes. This requirement is the same for panelized PWB's but the holes may exist on the breakaway material. The location and clearances are as in Figure 2.6. For SMT Assembly machine there is a location pin restriction of .400 area from front edge of Board or Pallet. See figure 2.6.A

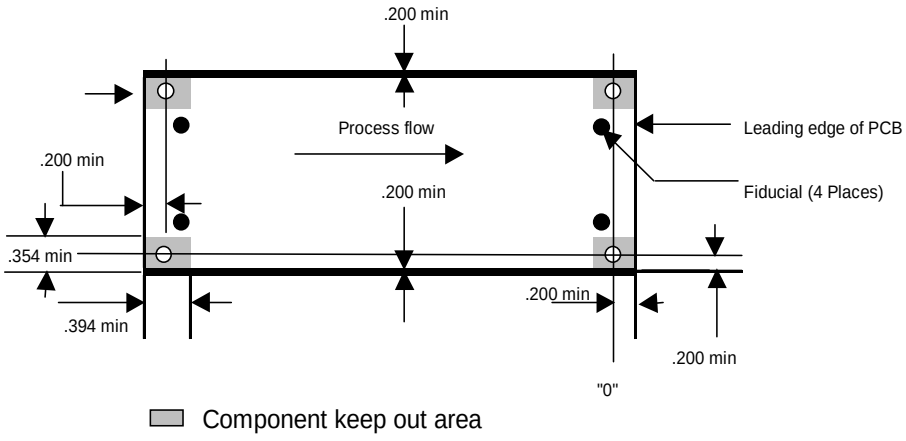


Figure 2.6: Tooling Hole Clearances and Placeable Area for SMT

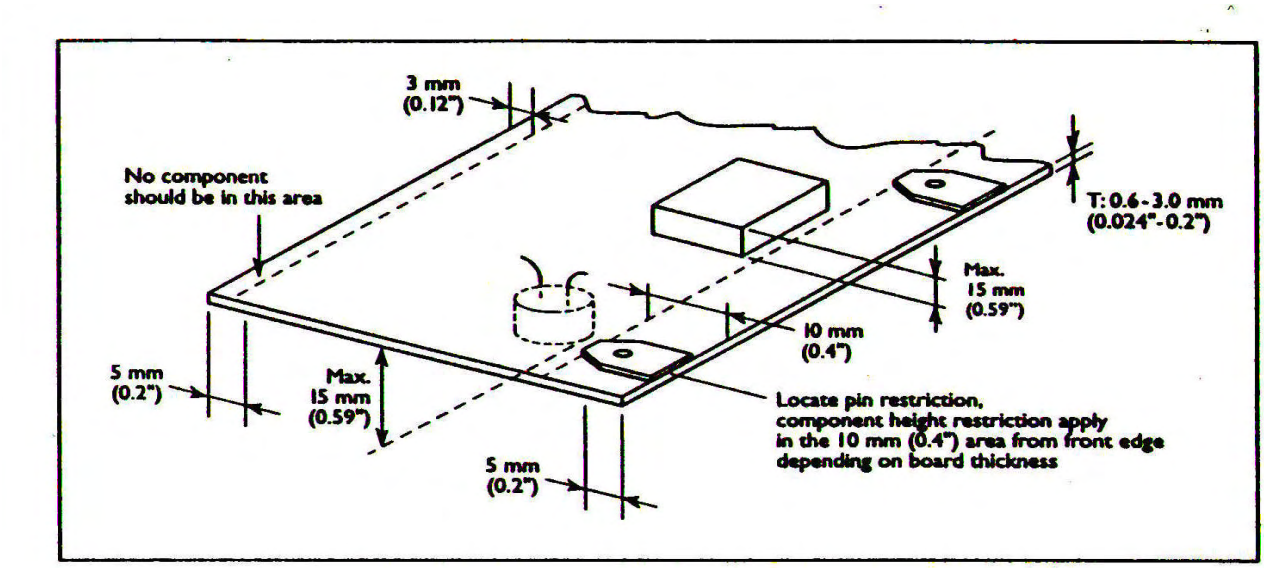


Figure 2.6A Mountable area for SMT assembly machine

2.7 Fiducial Marks – For each side of the PWB that has SMT components located on it, the PWB must have three global fiducials and one bad sense mark fiducial on it. No solder mask is allowed to cover these locations. The Fiducials should be placed as far apart from one another as possible on grid with respect to datum. For panelized boards, four fiducials on both sides are required on the breakaway material as well as each individual circuit in the array. See Figure 2.7 for locations and clearances.

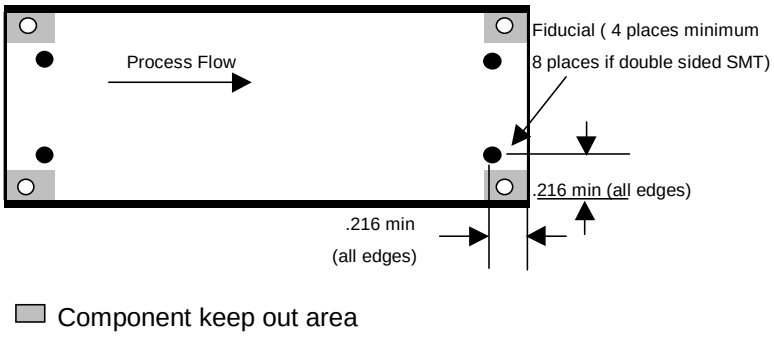


Figure 2.7: Fiducial Mark Locations

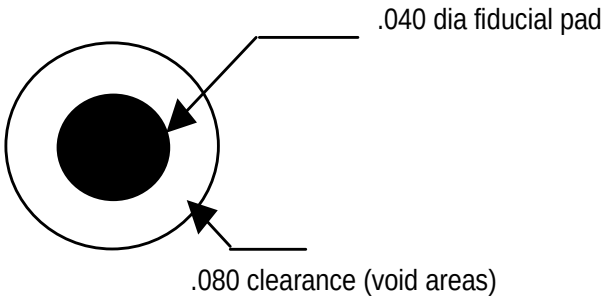


Figure 2.7.1: PWB Fiducial Marks

2.7.1 Global Fiducials–The preferred global fiducials are a .040" diameter with a .080" diameter window clear of silkscreen, solder mask, holes, or circuitry on outside layers. Fiducial marks may be required on stencil artwork for gluing on bottom side components. These are the same as bad sense marks.

2.7.2 Local Fiducials – All fine pitch patterns (.031 lead pitch or smaller) must have two local fiducials. (See Figure 2.7.2). These fiducials will be located on opposite diagonal corners of the land pattern so as not to allow the body of the device to infringe on the fiducial keep out area. The fiducial pads size is the same as global fiducials. Do not put fiducial openings in the solder paste stencil A/W.

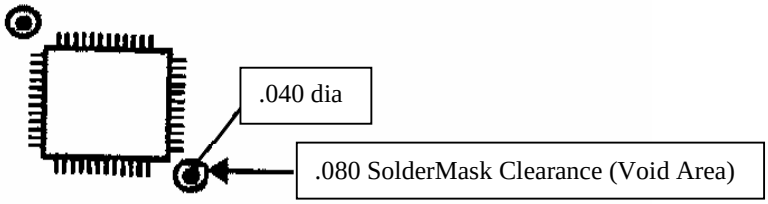


Figure 2.7.2: Component or Local Fiducial Marks

2.7.3 Bad Sense Mark – Smt layers will carry a .100 fiducial with a .100 minimum soldermask relief for machine requirements, quantity one per board, on each side top and bottom. Locate at edge of board outside component placement area.

2.8 Irregular Shaped Boards – PWB's with irregular edges should either have breakaway material added to the leading edge or be panelized to make the edge square (i.e. uniform and continuous). The leading edge of the board must be continuous as this edge needs to hit board stops in the SMT auto-placement machines and as it rides in on the finger conveyor system on the wave solder machines. See Figure 2.8.

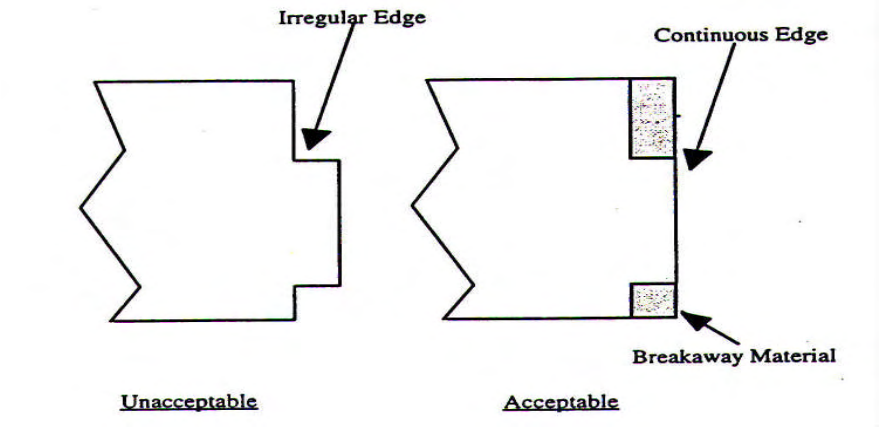


Figure 2.8: Irregular Shaped Boards

2.9 Panelization of PWB's – The following are guidelines for the panelization of PWB's. Boards with a minimum dimension smaller than 4.00 are candidates for panelization. The design engineer should consult with Colonial Electronic Manufacturers' Technical Director for inputs in order to meet the guidelines for assembly equipment.

2.9.1 Board Outline – Where possible, the shape of a panelized PWB should be square or rectangular in nature. This allows, for more economical material use than boards with complex shapes and projections.

2.9.2 Panel Size – Standard panel sizes are 12 x 16, 14 x 16, 16 x 18, 16 x 21, and 18 x 24. Preference is to use a standard 18 x 24 panel size to keep board yield high and cost low. Plateable area around panel requires .50 inches for Two sided material, and .75 inches for multi layer material.

2.9.3 Routing Tabs/Locations – The width of the route tab should be .100 max. One tab should be provided for every 3.0 of board edge length. Tabs should be placed from .5 to 1.0 from corners of the board in both directions. There should be at least 2 tabs for each side of the board that is 2.0 or greater in length. Route tabs are not allowed to be placed directly on corners. Tabs should not be located directly beneath overhanging components (connectors, etc.). All route locations should be defined on the fabrication drawing. See Figure 2.9.3.

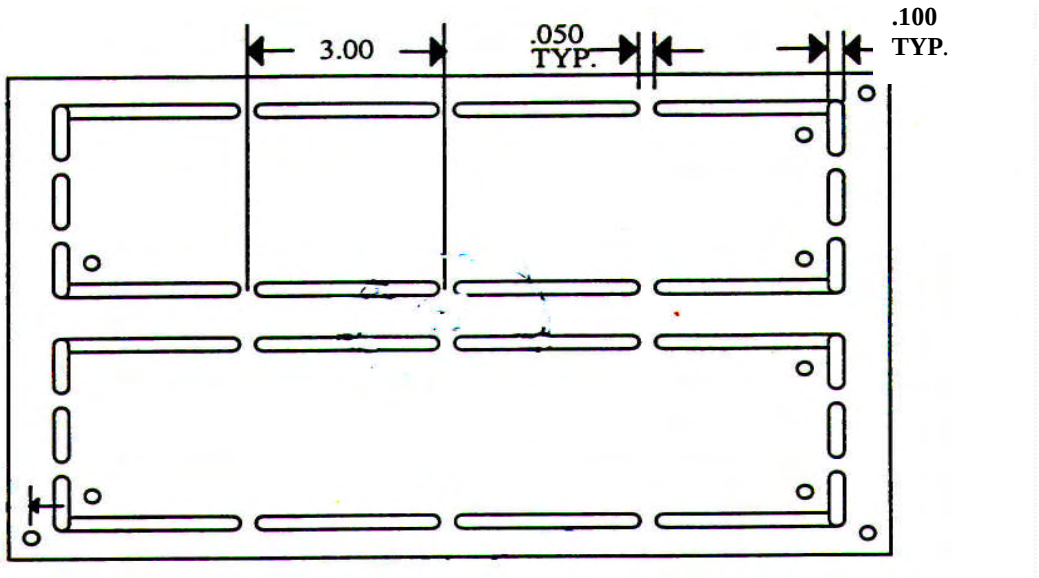
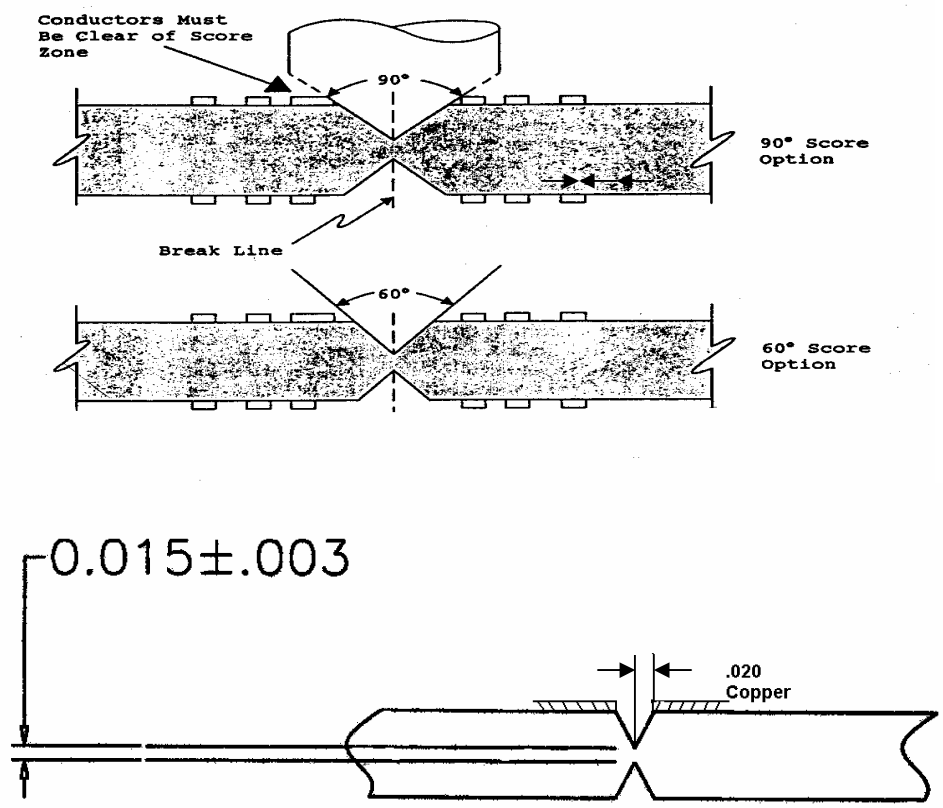


Figure 2.9.3: Panel Routing Specifications

2.9.4 V-Score Breakaway – The preferred V-scoring of a pallet will specify remaining material after cutting. Scoring locations and depth may vary depending on component weights, width going thru solder machine. Standard is .015 +/- .003 dimension. On board designs no outer or inner Copper layer will have copper present at V-score due to blade cutting into board edges. Never will exposed copper be allowed after individual Board is broken from pallet. Allow .020in from edge of board to any copper.



V – Score dimension consideration Figure 2.9.4

2.9.5 Micro-Drilling Breakaway Tabs – The preferred method of employing breakaway tabs is the use of micro-drilled breakaway tabs conforming to Figure 2.9.5. These tabs should occur approximately every three inches of breakaway Material. Use of this method will result in a burr free edge.

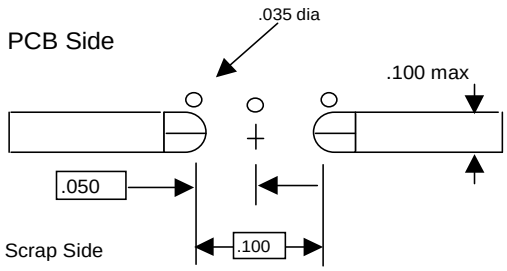


Figure 2.9.5: Micro-Drilled Breakaway Tab

2.9.6 Minimum Panel Margins – The minimum width of panel margins from an outer panel edge to the nearest breakaway slot is .500.

2.9.7 Step and Repeat Dimensions – For automatic test purposes, locate the same features on adjacent boards in even increments of .100 from each other so that the test points/vias can fall on an even grid.

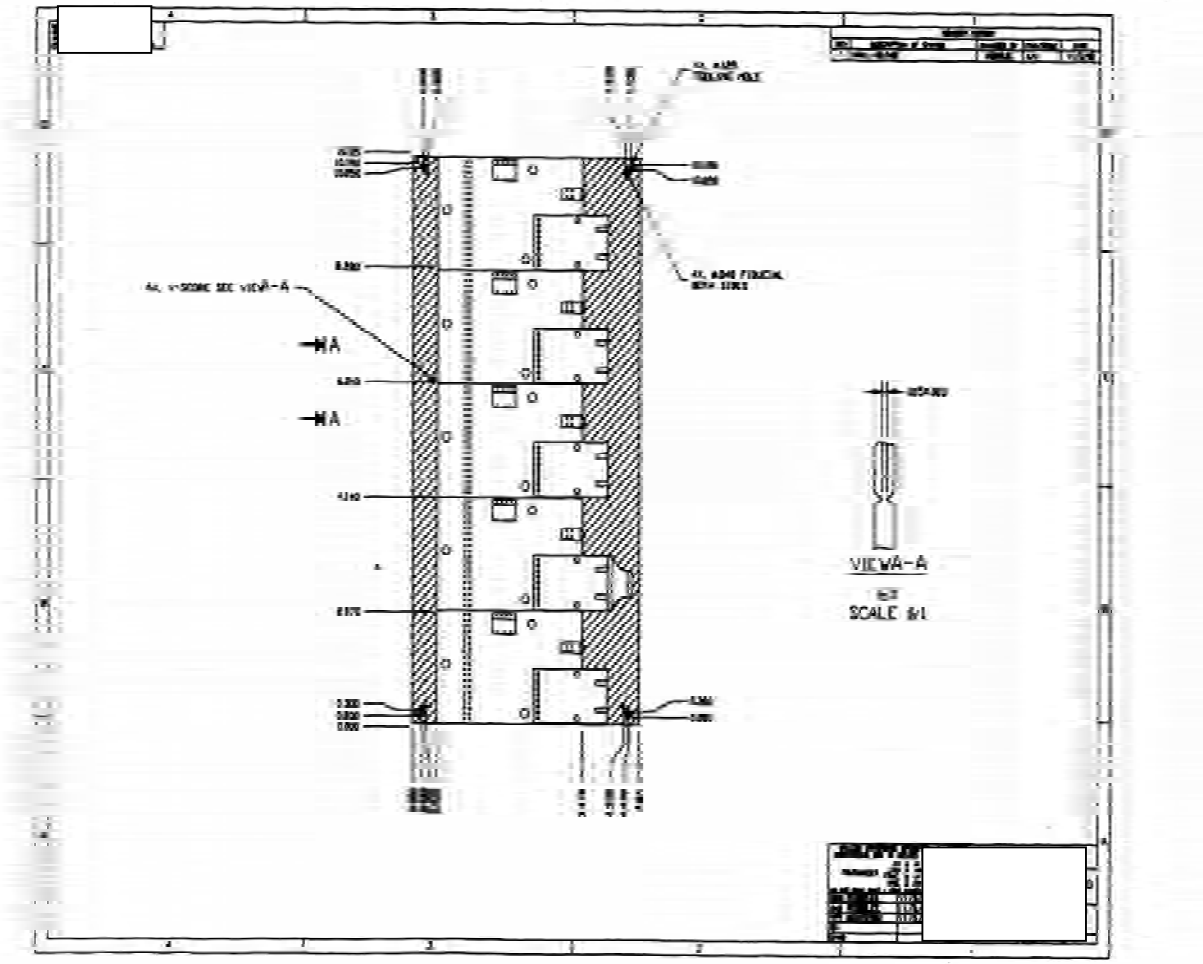
2.9.8 Wave Solder Support Slot – For each panelized board exceeding 12 inches in width design consult with Colonial Electronic Manufacturers' Technical Director to determine if there should be provisions for a support fixture. This feature is important for panelized boards due to the sagging possibility during the wave solder process.

2.9.9 Edge Connector Fingers – For PWB's requiring gold plating of edge fingers the panelization process may not be able to be utilized. The panelization technique is able to be utilized for tin/lead plated fingers. If a board with gold fingers is to be panelized the fingers must be on an outer edge for plating. Consult manufacturing engineering from your PWB supplier for gold plating process requirements.

2.9.10 Impeadance Control – On multi up panels for impeadance control boards, allow a .75 x 6.00 inch coupon in center of panel. Reference

registration coupons per IPC-D-275 designs standards for rigid boards.

2.9.11 Breakaways with overhang Components - Show breakaways cross-hatched to distinguish breakaway material versus usable board material. Show one board on pallet with component outlines that extend into the breakaway area. This makes it easier to visualize what can and can't be done for changes that can possibly reduce costs at the fabrication and assembly suppliers. This will represent the total overhang in relationship to the edge of the pallets for wave solder finger conveyor considerations.



2.10 Grids

2.10.1 Through-Hole Mounted Components – The preferred component mounting grids will be .100 for through hole components with respect to the x,y datum lines specified on the fabrication drawing. An .050 grid is acceptable but not preferred. Hole patterns that cannot be fit on grid should have at least one of their holes located on grid. It is preferred to have via holes fall on grid, especially if they might be used as converted test vias.

2.11 Artwork (Gerber .pho files) Generation

2.11.1 Silkscreen Artwork – A pattern showing coverage of reference designators and component body outlines that will be placed over the soldermask for identifying component body outlines and reference designators.

2.11.2Gerber Artwork – 1/1 scale photo plots of all PWB copper layers, solder masks, Solder paste stencils, and silkscreen.

2.11.3 Solder Mask Artwork – A pattern showing coverage of all copper conductors to be free from soldering.

2.11.4 Solder Paste Stencil Artwork – A pattern of openings in the solder stencil through which solder paste is deposited to the component pads.

2.12Silkscreen Considerations

2.12.1 – Silkscreen "Made in USA" flag symbol – If your product is completely assembled in the U.S.A. then the addition of a Made in U.S.A. and Flag symbol is a desirable option. This could Be added to the silk screen at no additional cost (provided that the board is still in the design stages). Or a label can be added after assembly is complete. The later would require a cost of labor and labels.

2.12.2 Silkscreen outline for Serial Number / Bar Code Label – If serial numbers or bar codes are required the area to receive the label should be marked on the silk screen layer, and represent the actual size of the label.

2.12.3 - Silkscreen component pin 1 and Polarity identifiers - All components having a pin number 1 or polarity identifier will be shown on the silkscreen and will be visible after component attachment.

2.12.4 - Identification – Artwork should contain the PCB part number. The PCB part number should be on the top side of the PCB with the current revision.

2.12.5- Silkscreen CE mark – CE and UL markings can be added to the silkscreen layers to reduce cost of labor and labels. Care must be taken to assure proper specifications are followed to meet requirements.

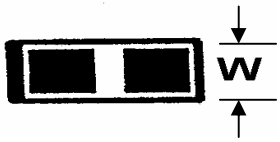
CE

Minimum Height = .20
Width = .28
Line Width = .03

2.12.6- Silkscreen Component Body outlines 0603,0805,1206

There are many ways to mark and identify components. The following are the minimum requirements for component identification. All 0603, 0805, and 1206 surface mount components will have the outlined identified as a .015 solid dot centered between the pads. All Tantalum Capacitors with case sizes of A,B,C and D will adhere to specification provided. The positive side will be identified with a double line width of .020. The body outline will be .010 line width. The silkscreen width of all bodies will adhere to the actual width of the component.

For 0603,0805,1206



Tantalum caps cases A,B,C,D
Case A width = .070
Case B width = .118
Case C width = .137
Case D width = .181

2.13 – Drill Drawing Information

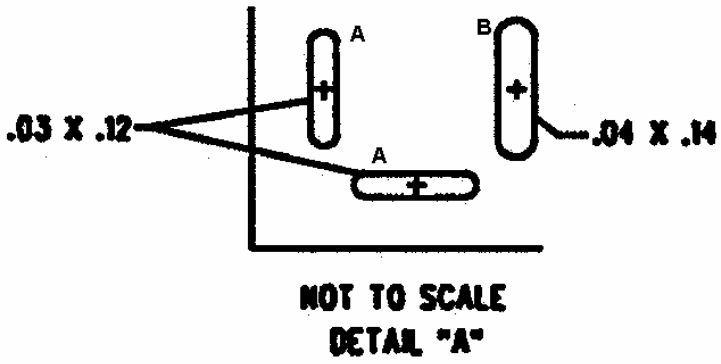
2.13.1 Drill Chart Hole Sizes - Drill chart will combine any hole sizes that overlay within specified tolerance range. Smallest size to be .013. Smaller hole size will go to next higher hole size as long as min +.007 over max MFG lead is obtained.

Examples; if Qty 33 with size .037 +/- .003
and Qty 10 with size .040 +/- .003
combine to Qty 43 with size .038 +/- .003

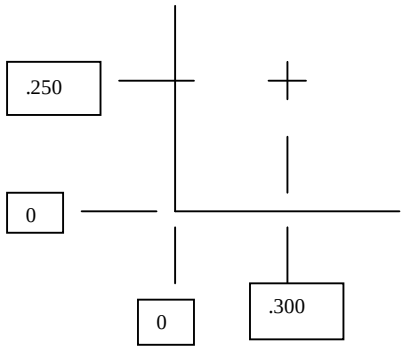
SYMBOL	SIZE	QTY	PLATED TYPE
+	.013 +/-.003	236	PLATED
×	.037 +/-.003	33	PLATED
⊡	.045 +/-.003	4	PLATED
◇	.062	2	PLATED
⧖	.071	4	PLATED
A	.030 X .120 SLOT	2	PLATED
B	.040 X .140 SLOT	1	PLATED
C	.115	2	PLATED
D	.118	1	NON-PLATED
E	.125	2	PLATED
F	.128	2	NON-PLATED

Fig 2.13.1 Drill Chart

2.13.2 Slots – Slots will be identified with a letter symbol and will have a detail "A" called out. This gives the PC fab supplier a clear orientation of slots. All slots will have an associated drill chart symbol referenced in the detail view.



2.13.3 Reference X-Y hole to edges – Drill drawing will identify one hole to two edges of board to accommodate PCB fabricator to locate corner of board for step and repeat associated with palletization, and routing of board edges.



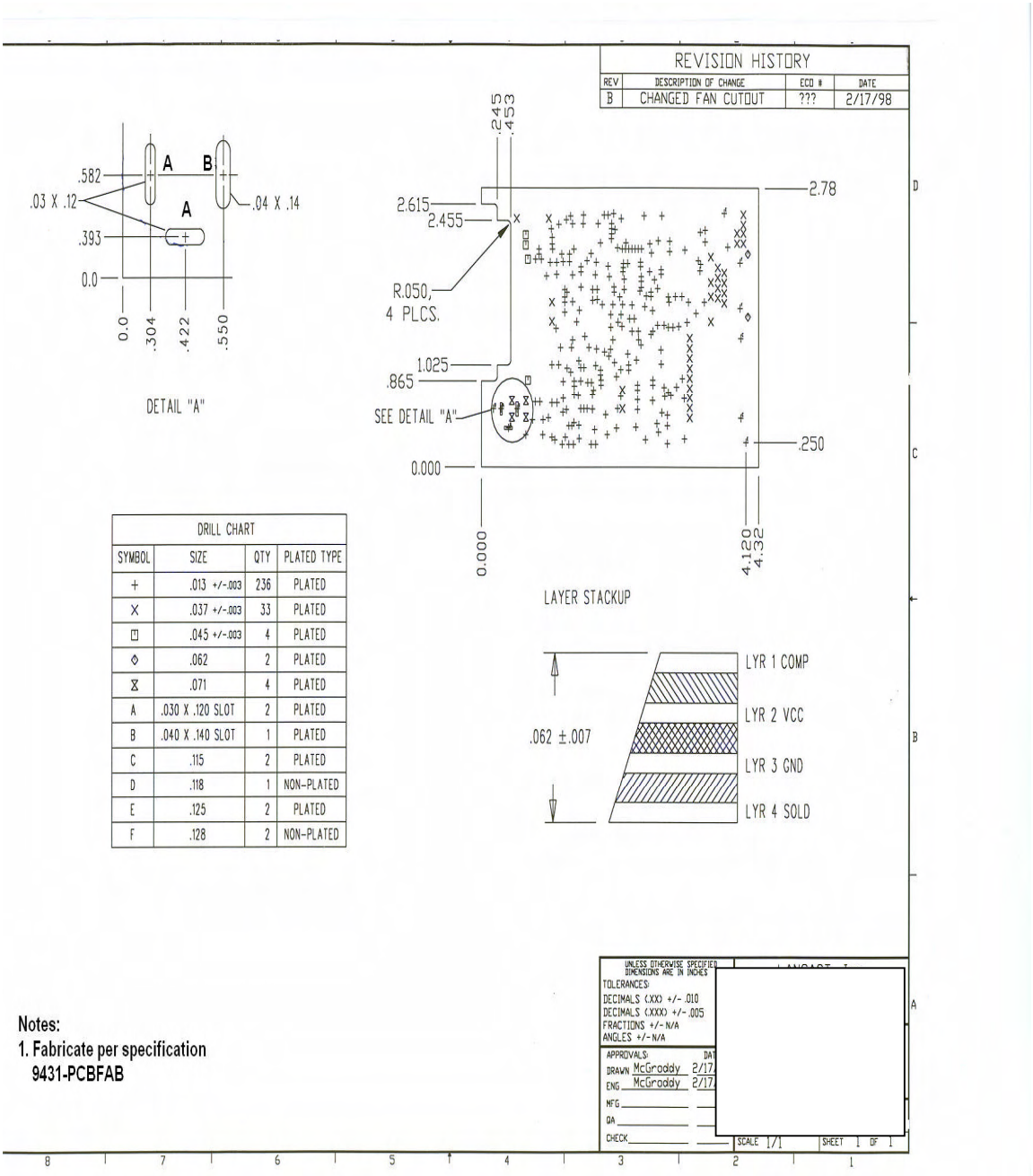
2.13.4 Standard drill drawing notes – All drill / fabrication drawings will carry these notes.

1) **Any exceptions to specifications will be listed as a note on drawings. Example: Gold plate Fingers**

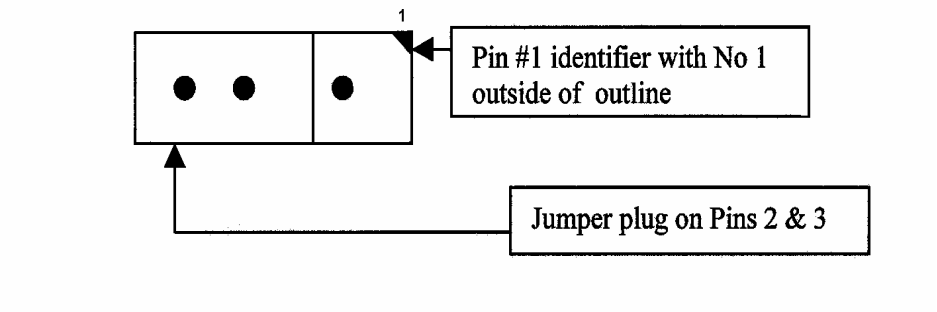
2.13.5 Chamfers – Chamfers on insertion type PCB's will be .02 x 45 degree both sides.

2.13.6 Standard routing bits – Standard routing bits are .100, .125, .093, and .062. Less than .062 will increase cost (10 to 20%). Specify a standard .100 routing bit.

2.13.7 Multi – layer stack up, tolerances – The drill / fab drawing will indicate the layer stack up and tolerances as shown;

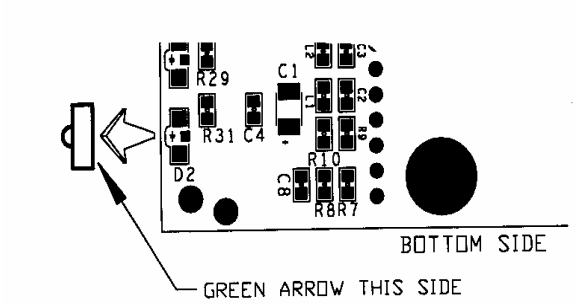


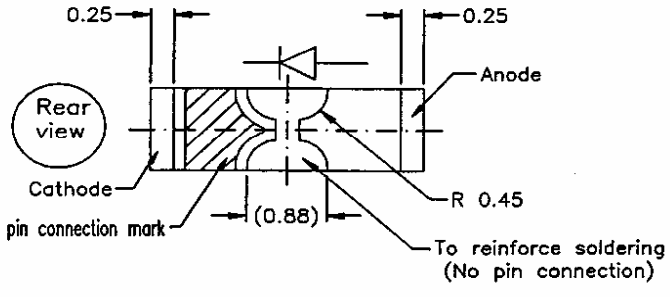
2.14 Assembly drawing information – Any notes, details or special instructions to make the assembly clear will be noted on the drawing. Any jumper plugs for jumper pin headers will be noted as such

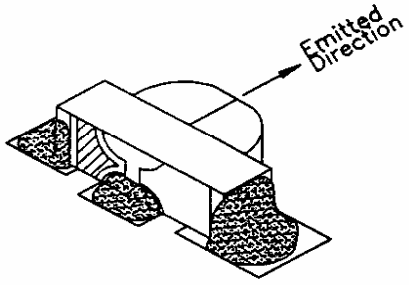


2.14.1 Find Numbers – Use of a find number (balloon item number) on drawing will be used whenever necessary such as hardware.

2.14.2 LED's – Any LED's having a colored mark on body to identify cathode end will be noted as such.







3. Mounting Example

2.14.3 Component locations – All components will be identified by the silkscreen reference designators outline.

2.14.4 Standard Note: Colonial Electronic Manufacturers Inc., as a default, will assemble to the guidelines of IPC-610-C, unless requested by the customer to assemble to the specifications of some other guideline.

2.15 Design Rule Check – All PCB designs should have a DRC performed for

- **Minimum copper width.**
- **Minimum spacing requirements.**
- **Silkscreen on component pads.**
- **Minimum annular rings on drill pads (components, vias, and mounting holes).**
- **Solder Mask clearances and coverage.**
- **Solder Paste openings.**

2.16 Cad Outputs

- **For a current sample of cad format needed for programming please request a sample from Colonial Electronic Manufacturers Inc. Technical Director.**
- **Aperture lists should include dcode, shape, quantity. No unused apertures will be included.**
- **X-Y programming of surface mount components should be in a column format preferably in an excel spreadsheet, clearly readable for programming input to machine. See example at the end of this handbook.**
- **Paper plots should be right reading for bottom copper layer and silkscreen layer for ease of checking design.**

3.0 PWB Design Considerations

3.1 Component Holes, Pads and Via Sizes

3.1 .1 Calculating Sizes (Holes and Pads) – Minimize the quantity of different hole sizes. Avoid sizes overlapping in tolerance. See Table 1 for the method of calculating hole and pad sizes. Note: Check manufacturers part specification for recommended hole sizes.

	Non-Plated Thru-Holes	Plated Thru-Holes
Finished Hole Size: Hand Inserted Part	N/A	L + 0.007 min
Auto Inserted Part	N/A	L + 0.012 min
Pad sizes External and Internal: External Layer Pad Size	H + .050 Min	H + .020 Min
Internal Layer Pad/Size Clearance	H+ .020 Min	H + .031 Min
Finished Via Sizes: .062 Thick PWB	Minimum Size = .013 + .000/-.008 with .030 ext pad size Preferred Size = .020+/-.003 with .040 ext pad size	
.093 Thick PWB	Minimum Size = .020+/-.003 with .040 ext pad size Preferred Size = .030+/-.003 with .058 ext pad size	
.125 Thick PWB	Minimum Size = .025+/-.003 with .053 ext pad size Preferred Size = .039+/-.003 with .068 ext pad size	

L = Part Maximum Lead diameter, H = Maximum hole Size
Maximum takes into consideration Manufacturers Tolerances

3.1.2 PTH Diameter Tolerance – For PTH's the specified tolerance should be as follows

	Hole Size	Tolerance
Equal to or Less than	**.061**	**±.003**
Equal to or Greater than	**.062**	**±.005**

3.1.3 Pads - The minimum via hole size is limited by PCB fabrication capabilities. It is preferred that no unused pads without traces be located on inner layer

3.1.4 External Pad Sizes for PTH's – See Table 1 for pad sizes and shapes on component and solder sides. For unlisted PTH pad sizes, pad diameter should be at least .020 larger than the associated nominal hole size.

3.1.5 Internal Layer Pad Size for PTH's – The internal layer pad diameters should be at least .031 larger than the associated nominal hole size.

3.1.6 Internal Layer Pad Sizes for NPTH's – A clearance should surround non-plated holes on all inner layers. The clearance should be of a size and shape to provide clearance of at least .020 larger than the nominal hole size where a no connect is desired.

3.1.7 External Layer Pad Sizes for NPTH's – A void should surround non-plated holes on all external layers. The void should be a size and shape to provide clearance of a least .050 larger than the nominal hole size where a no connect is desired.

3.1.8 Thermal Relief Pads – On Multi-Layer Boards, thermal relief pads should be used around all holes in voltage and ground planes where planes are connecting to IC's, resistor networks, and discrete components rated at one watt or less. The thermal pad is circular in nature split up into four sections with .010 to .020 between ends of the sections. The inside diameter for the thermal is .060 while the outside diameter is .080 for .038 plated through holes. The thermals should be at a 45° or 90°.

3.1.9 Converted Thermal Relief Pads –Internal voltage and ground connections from a cad output thermal shape can be converted to a direct hit to the internal plane by modifying the aperture list and noting the shape as "DH".

3.2 Circuit Layout

3.2.1 Preliminary Engineering Layout – Engineering study will determine initially the critical components on a given design from the standpoint of component density, heat dissipation, vibration factors, electrical compatibility, assembly, maintainability, and other functional requirements such as circuit frequency and speed.

3.2.2 Conductors

3.2.3 Distribution – Copper distribution on each layer should be as even as possible for proper copper etching, copper plating Balancing , and PWB Lamination warpage control. Outer layer conductors, side to side, should also be balanced. Open areas on internal layers should be filled with either additional power planes, ground planes or non-functional copper to assist in plating density fabrication concerns.

3.2.4 Minimum Line Width/Spaces – Utilize standard technology wherever possible to provide the highest yield and quality manufacturable PCB. However, use of fine line technology may be used if layer reduction can be achieved or space is at a premium

Technology	Line/Space	Tolerances
Preferred Technology	.008/.008	±.0015
Standard Technology	.006/.006	±.0015
Fine Line Technology	.005/.005	±.0015

3.2.5 Copper Thickness – All copper weights will be specified on the Drill / Fabrication drawing .

1/2oz = .0007 1oz= .0014 1 1/2oz = .0021 2oz= .0028

3.2.6 Signal Routing – On boards using through hole mounted dips, it is preferred that the signal runs on the solder side shall run perpendicular to the major axis of the dip. This allows signal runs between the lead mounting holes and permits an outward or inward crimp on the lead without danger of solder bridging to adjacent runs (if solder mask is not used). Where possible, signal conductors should be uniform in width along the entire conductor run using 45° cornering for FCC emissions.

3.2.7 Conductor Width – The minimum conductor width on the finished board should be determined on the basis of the current carrying capacity required, and the maximum permissible conductor temperature rise. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the board will be used. Charts for this purpose are available in IPC-D-275.

3.2.8 Conductor Length – Minimizing the length of conductor runs should be standard practice. This will result in the minimization of capacitance important in high frequency applications and minimizing ohmic resistance for critical voltage regulation requirements.

3.2.9 Conductor Bends – To minimize entrapment of processing chemical and FCC emission control, bends should be as indicated below.

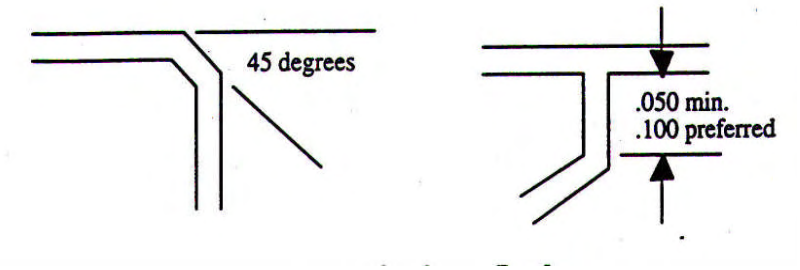


Figure 3.2.9: Conductor Bends

3.2.10 Conductors Routes Into SMT Pads – Conductors can be routed into a SMT land pad from any direction and from any angle, however circuits connecting to a pad may not lay beside the pad, which will effectively widen the pad. See Figure 3.2.10

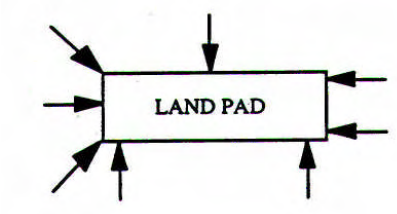


Figure 3.2.10: Conductor Routes Into SMT Pads

3.2.11 Spacing of Conductors to SMT Land Pads – Conductor should be spaced a minimum of .006 from a SMT land pad to allow for complete coverage of the conductor with solder mask. See Figure 3.2.11

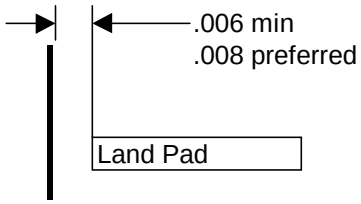


Figure 3.2.11: Conductor Spacing to SMT Land Pads

3.2.12 Edge Clearance – Unless the CAD outline drawing dictates otherwise, the following nominal dimensions (prior to fabrication and assembly tolerances) shall be the closest that components, mechanical parts, conductors, pads, and etched markings can be to PWB edges (exceptions are critically located parts such as connectors, LED's, switches, etc.).

Item	Edge Clearance
Conductors, pads, and etched markings on card guide edges.	External Layers - .150 inches Internal Layers - .025 inches
Conductors, pads, and etched markings.	Internal/External Layers - .025 inches
Edges of components and mechanical parts conveyor edges.	.125 inches minimum
Test Pads to Edge of Board	.125 inches minimum

3.2.13 Layer quantity and Voltage/Ground Plane Locations – To ensure board flatness, Multi Layer Boards will contain an even number of layers. Voltage and ground layers should be located at the center of the MLB lamination. To increase to an even number of layers if the design would have an odd number, the ground layer may be duplicated, with the duplicates located adjacent to each other. If the design contains a voltage layer, the two duplicate ground layers should sandwich the voltage layer. There should be no large bare board or large unbroken copper areas (greater than approx. 1 sq. in.) on internal or external signal layers. Cross hatching is recommended to fill in these areas and to break up large copper areas.

3.2.14 Repetitious Circuitry – When practical, component arrangement in circuits repeated on a particular PWB should be identical. If possible, functional circuits of mostly discrete components within a PWB should be physically separated for visual identification. See Figure 3.2.14

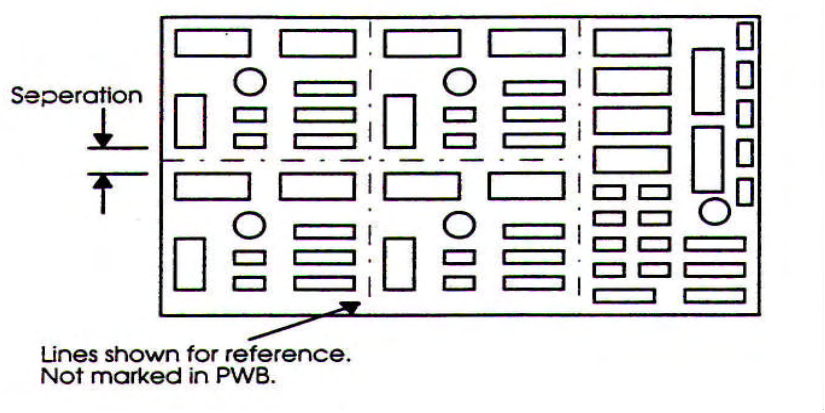


Figure 3.2.14: Repetitious Circuitry Sample

3.2.15 Reduction of Radio Frequency Interference/EMI – To produce EMI quiet design the rules layout below should be observed. In today's fine pitch and power "thirsty" LSI devices coupled with high speed clocks and SMT components (increased density per sq. inch) correctly placed devices and proper routing will result in better design.

3.2.16 Power and Ground Carrying Conductors and Vias – The via should be placed at the minimum distance as outlined in Figure 3.6.5. No thermal relief is required for the via. Only one power pin (VCC or ground) is allowed to be connected to the single via). The via can be shared by the bypass capacitor placed next to the power pin. The maximum width conductor should be used for power connection. The preferred vias for power and ground should follow preferred hole and pads listed in Table 2.4.

3.2.17 Decoupling Capacitors – The decoupling capacitor should be uniformly distributed throughout the board. At least 1 (one) bypass capacitor per power pin should be placed on the board in the proximity of VCC power. Any additional filtering or bypassing in an excess of standard by-pass should follow manufacture recommendation.

3.2.18 Chassis Ground – The chassis ground etch should not overlap any of power or signal ground on any of the layers. When the edge of the PWB contains connectors that utilize shielding for EMI reduction, there should be chassis ground "plane" on at least 2 (two) layers, connected at least 1" apart and providing connection to attached panel, the chassis ground etch shall be exposed allowing attachment of other EMI gaskets, connecting springs, etc. to the back panel. The width of the chassis ground should be at least .375 thick. If the layout allows, a wider etch is preferred.

3.2.19 Power – On power boards, where high voltage potential exists, conductor spacing should follow UL 1950, IEC 950 spacing requirements. The conductors and spacing should be identified by the cognizant engineer prior to starting PCB layout.

3.2.20 Telecommunication Circuits – The circuits intended for attachment to the wide area telecommunication network like (ISDN, TI, PSTN) shall provide 3mm clearance between primary and secondary circuits. The area under primary telecommunication circuit shall be clear of any planes (ground, power, chassis) and no other signals, shall be laid out in that area.

3.2.21 Clock Lines – The clock lines should be identified by cognizant engineer prior to layout. The clock lines should be routed away from PCB side that contains any connectors interfacing with outside world. The component placement should minimize length of the clock. The clock should be routed in the daisy chain fashion, the "stubbing" should be avoided. There might be other constraints related to clocks those should be identified by the design engineer prior to routing. The preferred placement of clock lines is next to the ground plane layer.

3.3 Component Layout, General

3.3.1 Component Placement – All components should be laid out to utilize automatic placement and insertion equipment.

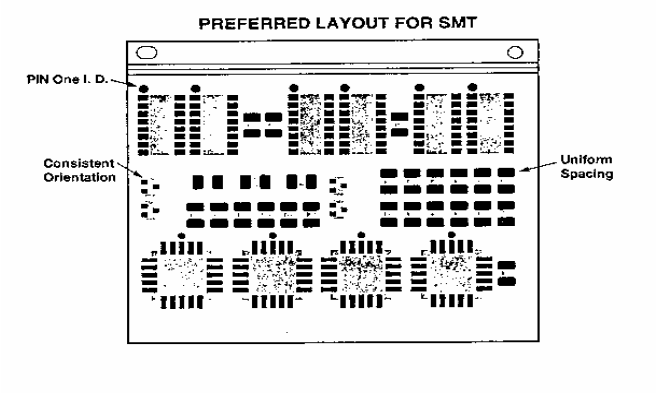
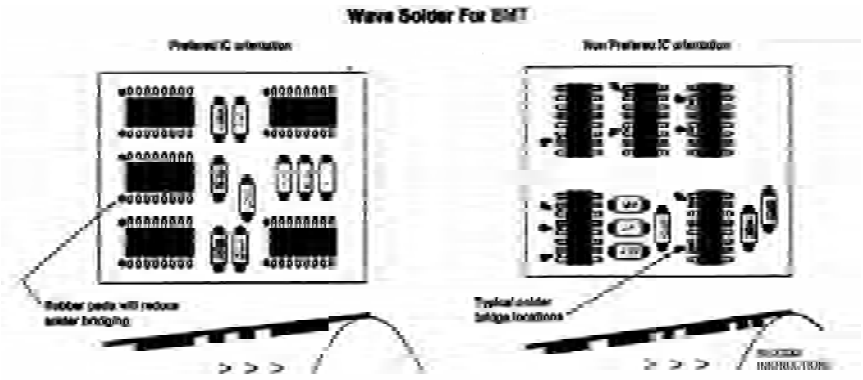


Figure 3.3.1 – Component Placement

3.3.2 Component Orientation for Wave Solder – The preferred orientation is used in order to optimize the resulting solder joint quality as the assembly exits the solder wave.

- **All passive components shall be parallel to each other.**
- **All SOIC's shall be perpendicular to the long axis of passive components.**
- **The longer axis of SOIC's and of passive components shall be perpendicular to each other**



3.3.3 Heat Dissipating Parts – Parts dissipating more than one watt or having an operating temperature of more than 240°F (115°C) should be mounted so that the body of the device is not in direct contact with the PWB surface unless appropriate heat sinking is used to lower the operating temperature within acceptable limits.

3.3.4 Component Contact and Obstruction – Components should not touch each other or mechanical parts, nor be stacked. No component should inhibit the ability to rework an adjacent part. This means be careful in the positioning of taller parts next to Through-Hole or SMD devices so as to allow adequate space for rework tools. This space should be .100 or larger.

3.3.5 Parts Sensitive to Shock and Vibration – Components susceptible to failure from shock or vibration should be located as near to the edge of the board mounting points as possible.

3.3.6 Components Within Board Area – No portion of a component should extend beyond the edge of the PWB, except designated parts on the CAD drawing (i.e. connectors, etc.)

3.3.7 BGA Components – Components must not be allowed within .200 around perimeter of device to allow for rework station nozzle clearance to keep rework of surrounding components to a minimum.

3.4 Component Alignment

3.4.1 Discrete Components – Unless design requirements dictate otherwise, discrete components mounted parallel to each other in a line should be lined up on their centers. It is preferred that all components be mounted in one-axis orientation, but two axis orientation is acceptable when required.

3.4.2 Component Polarization – All polarized components (or components with keying features, such as transistors) should be mounted with their indicated polarity ends or keying features facing the same direction throughout the entire design, or within circuit groups where possible.

3.5 Component Orientation

3.5.1 Top Side Component Orientation – Figure 3.5.1 shows the proper orientation for dual in line top side components.

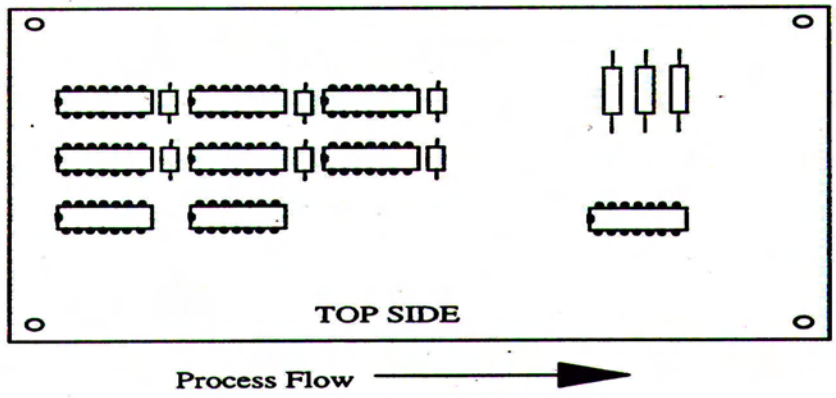


Figure 3.5.1: One Axis Layout Through-Hole

3.5.2 Bottom Side SMT Component Orientation – Figure 3.5.2 shows the proper orientation for bottom side components.

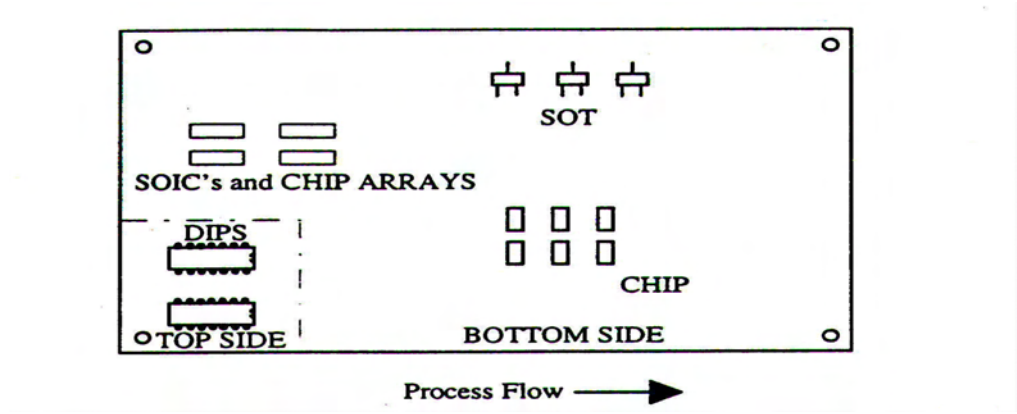


Figure 3.5.2: Bottom Side SMT Component Orientation

3.6 Clearance Requirements

3.6.1 Component Clearance for Socketed Dips and Axials – Figures 3.6.1 and 3.6.1A show the appropriate clearances to allow for automatic insertion of through-hole components.

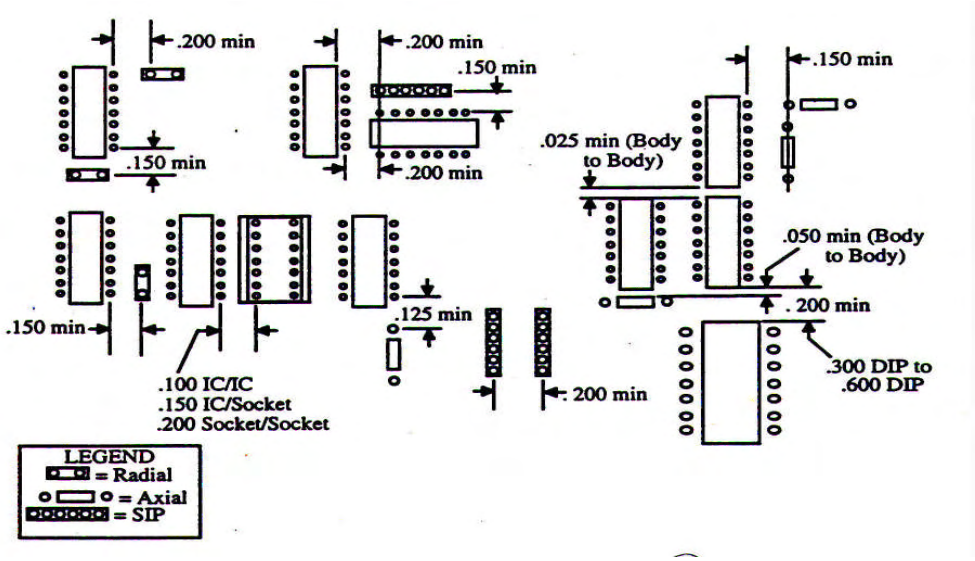


Fig 3.6.1 Component clearance for thru hole devices

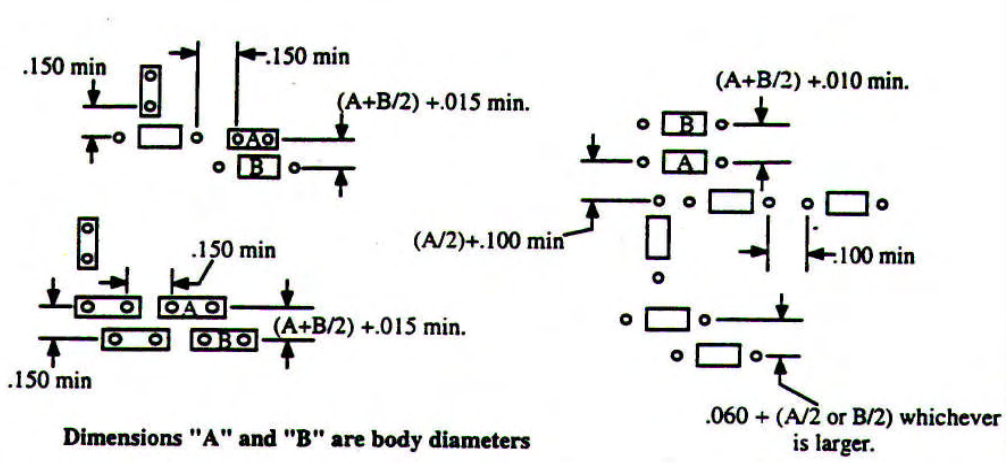


Figure 3.6.1A: Component Clearance for Axials and Radials

3.6.2 Axial and Radial Lead Hole Spacing for Automatic Insertion – Axial leaded hole spacing is equal to the maximum body length of the component plus .126 plus one nominal lead diameter for bend radius clearance. Maximum insertable lead to lead length is .600 and maximum body diameter is .200. Radial component lead spacing is .200 preferred. Transistor packages should be .100 lead to lead spacing with the leads being in line. Maximum transistor body diameter is .312 and maximum body height is .400.

3.6.3 Component Clearance Top Side SMT and T.H. – Pad to Pad – Figure 3.6.3 shows the appropriate top side SMT to SMT and SMT to T.H., pad to pad clearances.

Description	Spacing TopSide
Chip to Chip	.040 typ, .025 min
Chip to SOIC	.040 typ, .025 min
Chip to Tantalum Cap (cases A,B,C,D)	.040 typ
Chip to PLCC	.040 typ, .025 min
PLCC/SOJ to PLCC/SOJ	.100 typ, .050 min
SOIC to SOIC	.050 typ, .025 min
SOT23 to SOT23	.040 typ, .025 min
Chip to axial component body	.075 typ, .050 min
PLCC/SOJ to dip pad	.060 typ
PLCC SMT socket body to PLCC SMT socket body	.050 typ, .040 min
PLCC Socket body to other body if height is higher than socket	.100 typ, .075 min
Fine pitch to fine pitch	.100 typ, .075 min
Fine pitch to non-fine pitch (.020 pitch)	.250 typ, .100 min

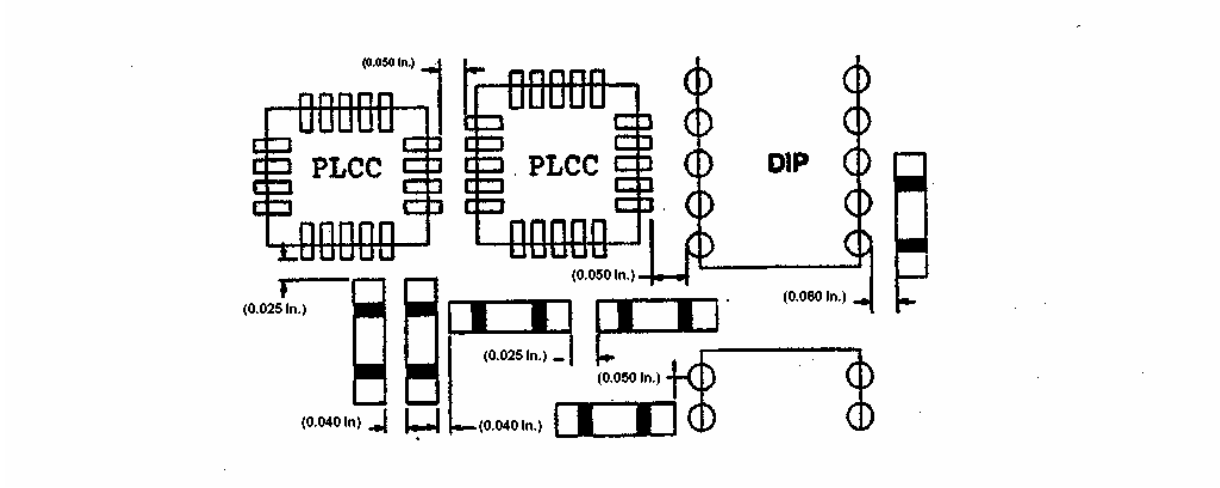


Figure 3.6.3: Component Clearance Top Side SMT and Through-Hole – Pad to Pad

3.6.4 Component Clearance Top side leaded and Bottom Side Thru hole – Pad to lead Figure 3.6.4 shows the appropriate Topside Through hole to bottom side SMT clearances.

Description	Spacing Bottom side
Chip to Chip	.040 Typ, .030 Min
Chip to Tantalum Capacitors (Cases A,B,C,D)	.050 Typ, .040 Min
Chip to SOIC	.050 Typ, .040 Min
SOIC to Tantalum Capacitors (Cases A,B,C,D)	.050 Typ, .040 Min
SOIC to SOIC	.050 Typ, .040 Min
Tantalum Cap to Tantalum Cap	.050 Typ, .040 Min

Fig 3.6.4 Component Clearance

3.6.5 BGA component spacing requirements – Fig 3.6.5 shows the appropriate clearances between component body and adjacent component. No components are allowed within .200 in around perimeter of BGA device. This area is reserved for rework equipment nozzle space requirements.

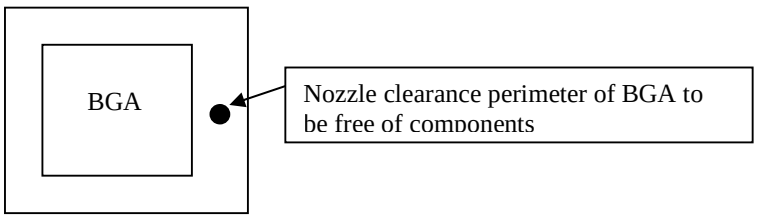
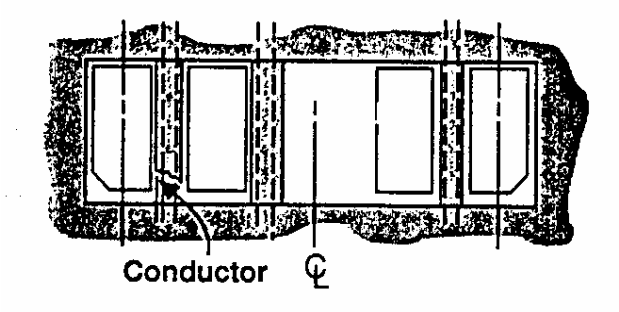
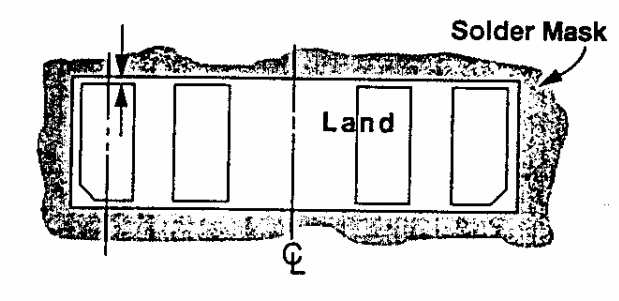


Fig 3.6.5 BGA Spacing

3.7 Solder Mask – Solder masks should be designed for both primary and secondary sides of the PWB. See below for clearances/coverage's. For fine pitch component pads a pocket soldermask is preferred. If pads cannot accommodate a minimum coverage of .004 then a gang soldermask is acceptable. All vias will be covered unless specified.



Pocket Solder Mask



Gang Solder Mask

Clearances/Coverage's

Area	Clearance/Coverage
Un-plated Holes, Slots and Cutouts	.050 Min. clearance around each hole.
Component Pads, Test Pads	.003 nominal/.0025 min clearance around each pad
Edge Fingers	The mask should stop at the ends of the fingers.
Traces adjacent to pads	Extend min. of .003 beyond edges of traces.
Between fine pitch pads	.004 min. coverage between pads.
Via Holes	100% coverage.

3.8 Surface Mount Land Pattern Design

3.8.1 Land Pattern Design Standards – Use the current IPC-SM-782 Surface Mount Land Patterns specification for all land patterns.

3.8.2 Bottom Side Actives and Chip Arrays – If necessary, bottom side chip arrays and SOIC's (50 mil pitch) can be designed onto the bottom side of the board and wave soldered, provided the maximum process temperatures are within the parts specifications. Leading and trailing pad width should be increased 100% for solder thieving.

3.8.3 SQFP and QFP (Square) land patterns – The total length and width of pad will be calculated using IPC-SM-782 subsection 11.2. When a QFP does not fit any component identifier listed the following table will be used to determine the width and length of pads.
The solder paste for pads will be equal to the land size.
The Soldermask relief between pads must be preferred .008, acceptable .006, minimum acceptable .004

Zmax = T + Jh Max + Jt Max
Xmax = W + 2 Js Min

Component Pitch	Toe Jt Max	Heel Jh Max	Side Jh Min
0.031	0.017	0.030	0.001
0.025	0.017	0.030	0.001
0.019	0.020	0.026	0.001
0.015	0.020	0.026	0.001
0.012	0.020	0.026	0.001

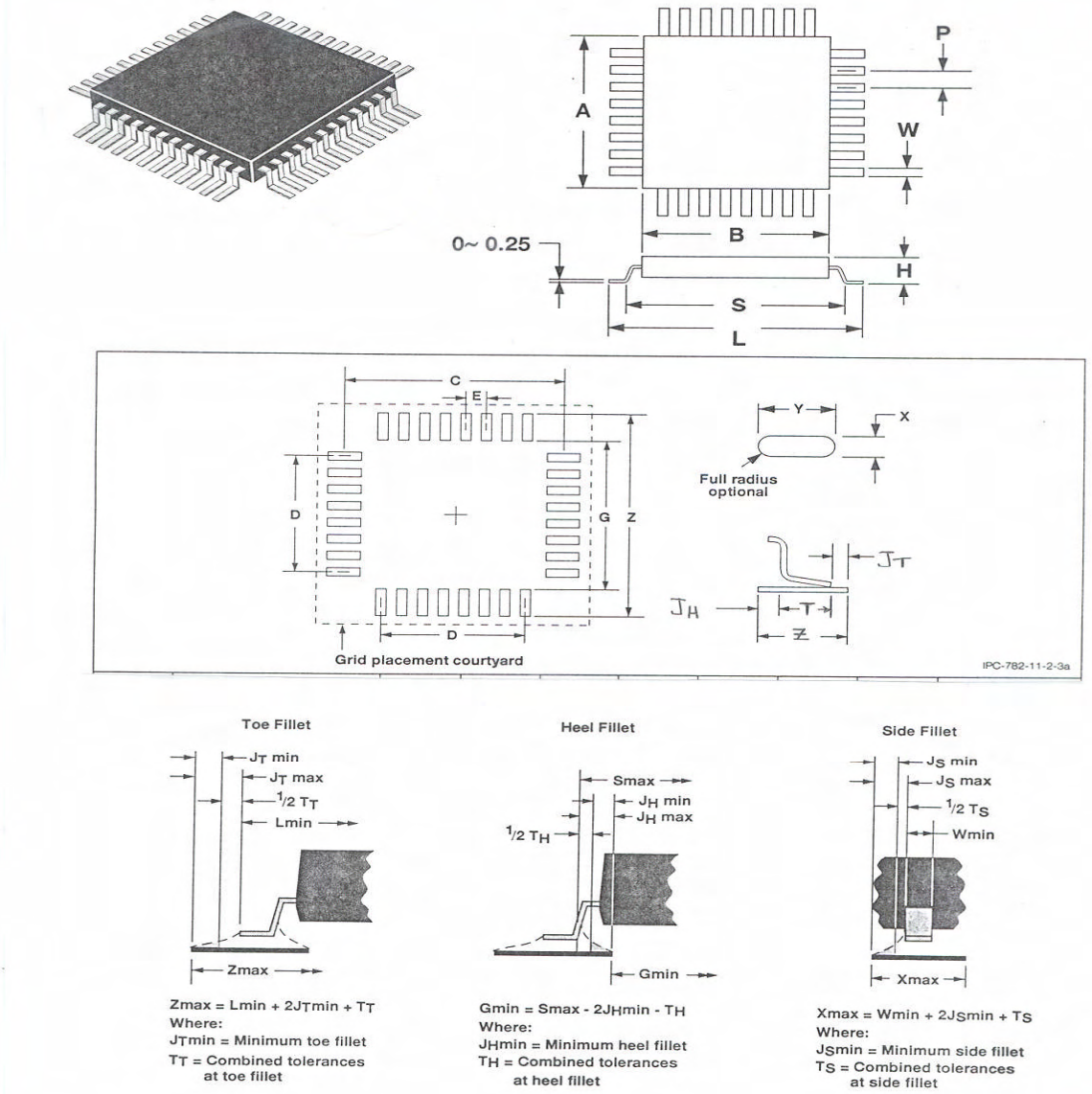


Figure 3.8.3 SQFP and QFP Land Patterns

4.0 Design for Testability

4.1 General

A) There must be at least one testable point per every electrical net except where that added track or capacitance from the via will degrade the electrical performance.
B) It is required that every node be accessible, and the primary means of accessibility should be a test pad. However, any net within a through-hole mounted device satisfies this requirement, since a through-hole mounting pad may serve as a test point.
C) There should be one test pad at each unused IC pin to facilitate library testing excluding mechanical alignment pins.
D) Every effort should be made to ensure that from spin to spin of the artwork, the pad locations will not change unless the designer specifically calls out for that to happen. There may be significant production delays and costs associated with moving test points.
E) All test pads must be placed on the bottom of the board. Drop in test pads outside of through-hole component outlines on all optionally loaded components.

F) Test-Pads should be as evenly distributed across the PCB as much as possible. Excessive pin densities in any one area will cause excessive board flex during test which can cause component damage. A maximum pin density of 50 pins per square inch is recommended.
G) Test Points should be placed as close to the OUTPUT of a device as possible with the shortest possible path. It is recommended that Critical Test-Pads be positioned and connected before routing begins.

4.2 Test Pads (General)

A) Test Pads grid is variable. The spacing, center to center, between the test points are preferred to be on .100 centers, .075 optional, .050 minimum, .025 optional, and must be solder coated.
B) Test points are preferred to have center to center spacing of .100. Test pads on .025 grids are possible but require the use of .025 probes which are more fragile and will increase the overall cost of processing.

4.3 Test Pad Masking and Location

A) Test points are to be free of solder mask and located on the bottom side of the PWB only.
B) Edge fingers, circuit traces or SMT lands are not to be considered test pads as they provide poor contact reliability and/or may provide a "false positive" test result.
C) All used and unused connector pins should be designated as a Test Point to facility 100% shorts testing of connectors.
D) Edge fingers that are not connected to an electrical net on the board (unused) need not have a Test Pad placed on the net if the ends of the fingers are to be solder masked during the wave solder process thereby eliminating the possibility of shorts between two adjacent traces.
E) Care should be taken not to place Test Pads near through hole component lands that may be bent over (clinched leads) in the manufacturing process.
F) Test Point/Pads should be placed at the end of a run of track on I/O's and optional RAM sockets, i.e. the last socket on the I/O bus or output connector, the last SIMM socket in a bank of RAMs.

4.4 Test Pads and Component Clearances

A) Test Pads should not be located too close to solder side components. The actual distance from the body edge of a solder side component to the edge of a test pad depends on the component's height. Follow the below guide for test point spacing from solder side components.

Clearance	Height of Component
.050 min.	<.075
.100 min.	>.075 but <.250
.200 min.	>.250

B) Test Pads will be preferred .040 minimum in size, and acceptable .035

C) Test Pads may be placed on traces as explained below. Please note that the minimum requirement for this method is the Test Pad must encapsulate 100% of the signal trace.

4.5 Test Pad/Via Combination – Vias may be used as Test Pads provided they meet the following criteria:

A) The converted via pad must be .040 diameter minimum with a preferred .013 max. plated hole.
B) Via's are preferred to be on .100 center to center spacing, if necessary .075, .050 and .025 with consideration of costs
C) No solder mask material on the Test Pad via.
D) Location to components must meet all the criteria outlined in Test Pads and Component Clearance section.

4.6 Power and Ground Test Requirements

A) At least four test points per ground and power planes evenly distributed across the PCB are required for proper power and ground distribution.
B) Power and Ground test points should be allocated such that no more than 300 mA of current is conducted through any one test point.
C) On dense SMT boards where power test pads are required, a larger pad is preferred (i.e. .060 diameter). This will allow for larger multi-point pins for better power transfer.

5.0 Deliverable checklists

5.1 Deliverables from PCB Design Cad Supplier:

PRODUCT NAME_____ REV LEVEL TO BE ASSIGNED____

1) **Photoplotting files to be submitted in Gerber Command Format.**
2) **Photoplot files to include Job Name and Revision.**
3) **Photplot files to have preferred composite Aperture report.**
4) **Assembly and Drill Drawing files to be in .DXF format for Autocad.**
5) **SMT Design land patterns and design rules per IPC-SM-782A Standard.**
6) **Silkscreen symbols such as: part number, CE mark and flag "Made in USA" logo should be included at this step.**
7) **All SMT parts on the bottom side of board are preferred to be placed parallel to the wave solder.**
8) **Any SMT parts on the bottom due to height will be placed to eliminating shadowing. Ref SM-782A courtyard outlines.**
9) **PLOT SCALING RATIO TO BE 1:1 UNLESS SPECIFIED**
10) **Naming of JOB FOLDER: product number and Revision.**
    Example: YYYYYYR1

FILE DESCRIPTION	FILE NAME
COMPLETE APERTURE REPORT FILE	YYYYYYAF.REP
ASSEMBLY DRAWING TOP	YYYYYYAT.DXF
ASSEMBLY DRAWING BOTTOM	YYYYYYAB.DXF
DRILL DRAWING WITH BOARD DIMENSIONS	YYYYYYDD.DXF
DRILL FILE NC (EXCELLON-COMPATIBLE FORMAT)	YYYYYYDR.DRL
DRILL TOOL FILE REPORT	YYYYYYDR.REP
SILKSCREEN TOP	YYYYYYST.PHO
SILKSCREEN BOTTOM	YYYYYYSB.PHO
LAYER 1 ARTWORK TOP SIDE OF BOARD	YYYYYYL1.PHO
LAYER 2 ARTWORK (MULTILAYER OR FOR TWO SIDED, BOTTOM SIDE OF BOARD)	YYYYYYL2.PHO
LAYER 3 ARTWORK (MULTILAYER)	YYYYYYL3.PHO
LAYER 4 ARTWORK (MULTILAYER, BOTTOM SIDE OF BOARD)	YYYYYYL4.PHO
LAYER_ _ _ _ ARTWORK (MULTILAYER)	YYYYYYL_.PHO
SOLDERMASK TOP SIDE	YYYYYYMT.PHO
SOLDERMASK BOTTOM SIDE	YYYYYYMB.PHO
PASTE MASK SURFACE MOUNT DEVICES TOP SIDE	YYYYYYPT.PHO
PASTE MASK SURFACE MOUNT DEVICES BOTTOM SIDE	YYYYYYPB.PHO
X-Y LOCATIONS FOR SMD PARTS ASCII FORMAT	YYYYYYXY.LST
Statistics on Layout, Connections, DRC, Padstacks, and Symbols	SUMMARY REPORT
JOB FILE ASCII FORMAT	YYYYYYJB.JOB

The **Deliverable package** will consist of Gerber files for all layers, NC drill file and report, Aperture report, Drill and Assembly Drawings in DXF format, 1:1 paperplots if requested by designer, Floppy disk with ZIPPED file and JOB file.

5.2 Deliverables to Fabrication Supplier. See checklist:

FILE DESCRIPTION	FILE NAME
APERTURE REPORT FILE	YYYYYYAF.REP/RPT/LST
SILKSCREEN TOP	YYYYYYST.PHO
SILKSCREEN BOTTOM	YYYYYYSB.PHO
DRILL FILE NC (EXCELLON-COMPATIBLE FORMAT)	YYYYYYDR.DRL
DRILL TOOL FILE REPORT	YYYYYYDR.REP/RPT/LST
LAYER 1 ARTWORK TOP SIDE OF BOARD	YYYYYYL1.PHO
LAYER 2 ARTWORK (MULTILAYER OR FOR TWO-SIDED,BOTTOM SIDE OF BOARD)	YYYYYYL2.PHO
LAYER 3 ARTWORK (MULTILAYER)	YYYYYYL3.PHO
LAYER 4 ARTWORK (MULTILAYER, BOTTOM SIDE OF BOARD)	YYYYYYL4.PHO
SOLDERMASK TOP SIDE	YYYYYYMT.PHO
SOLDERMASK BOTTOM SIDE	YYYYYYMB.PHO
STENCIL PASTE MASK SURFACE MOUNT DEVICES TOP SIDE	YYYYYYPT.PHO
STENCIL PASTE MASK SURFACE MOUNT DEVICES BOTTOM SIDE	YYYYYYPB.PHO
DRILL DRAWING	XXXXXX-XXXRX.dwg
PALLET DRAWING	XXXXXX-XXXRX.dwg
README TXT FILE (if applicable)	XXXXXX-XXXRX.txt

5.3 Deliverable to Assembly Supplier. See checklist:

FILE DESCRIPTION	FILE NAME
X-Y LOCATIONS FOR SMD PARTS ASCII DOS FORMAT	YYYYYYXY.LST
ASSEMBLY DRAWING TOP SIDE	XXXXXX-P1RX.dwg
ASSEMBLY DRAWING BOTTOM SIDE	XXXXXX-P2RX.dwg
BILL OF MATERIALS	XXXXXX-XXXRX
APERATURE (LIST) FILE REPORT	YYYYYYAF.REP/RPT/LST
APERTURE REPORT FILE	YYYYYYAF.REP/RPT/LST
SILKSCREEN TOP	YYYYYYST.PHO
SILKSCREEN BOTTOM	YYYYYYSB.PHO
STENCIL PASTE MASK SURFACE MOUNT DEVICES TOP SIDE	YYYYYYPT.PHO
STENCIL PASTE MASK SURFACE MOUNT DEVICES BOTTOM SIDE	YYYYYYPB.PHO
PALLET DRAWING	XXXXXX-XXXRX.dwg
README TXT FILE (if applicable)	XXXXXX-XXXRX.txt

EXAMPLE OF CAD DATA FORMAT FOR MACHINE PROGRAMMING.

Ref. Des.	Part #	Part Type	X Coord.	Y Coord.	Rotation	Top/Bot
C1	123-456	0603	1.250	3.125	0.0	TOP
R21	234-567	1206	2.250	5.500	90.0	TOP
Q2	859-712	0603	1.175	8.750	270.0	BOT
C22	758-821	0603	1.250	1.125	90.0	BOT
L1	357-956	1812	2.500	1.250	180.0	TOP

X-Y Data should include Fiducials and Bad Sense marks. Also step & repeat info if not already recorded on a pallet drawing.

Revision History			
Rev	Reason for change	Changed by	Date
A	Initial release	B. LeBlanc	3/7/00
B	1. Restructure CAD Data Format 2. Change global fids to PCB Bad Sense Marks. 3. Single local fid not acceptable	B. LeBlanc	5/4/00
C	Add Hole size to tooling hole requirements	B. LeBlanc	5/16/01